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EXAMINER	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICHAEL Y. LAI

Appeal 2009-005254
Application 10/674,364
Technology Center 2100

Before JAMES D. THOMAS, CAROLYN D. THOMAS, and DEBRA K. STEPHENS, *Administrative Patent Judges*.

C. THOMAS, *Administrative Patent Judge*.

DECISION ON APPEAL[1]

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134(a) from a final rejection of claims 1-57. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

According to Appellant, the invention relates to "compiling code for a network processor such that bit fields in the compiled code are processed efficiently" (Spec. 2, ¶ [0001]).

Claim 1 is illustrative:

> 1. A method comprising:
>
> generating an intermediate representation (IR) of a source program, where the source program includes one or more instructions for processing data in a bit field within a data structure;
>
> modifying the intermediate representation to more efficiently execute the one or more instructions for processing the bit field data; and
>
> generating resultant code based on the modified intermediate representation.

Rejection

Claims 1-57 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Tye (U.S. 6,226,789 B1, May 1, 2001).

GROUPING OF CLAIMS

Appellant argues claims 1-57 as a group on the basis of claim 1 (*see* App. Br. 11). We select independent claim 1 as the representative claim. We will, therefore, treat claims 2-57 as standing or falling with representative claim 1. *See* 37 C.F.R. § 41.37(c)(1)(vii).

FINDINGS OF FACT (FF)

Tye Reference

1a. Tye discloses:

> During translation, the background translator reads instructions in the first instruction set …, builds an intermediate representation (IR) …, and then modifies the IR to produce a final version of the IR that corresponds to instructions in the second instruction set. In the example …, the first instruction set is associated with a complex instruction set computer …. The second instruction set is associated with a reduced instruction set …. (*see* col. 63, ll. 16-26).

1b. Tye discloses: "One implementation of the IR uses a code cell as a basic atomic unit for representing instructions in the IR. The IR comprises one or more code cells connected." (col. 63, ll. 33-36).

1c. Tye discloses: "Referring now to FIG. 45[,] a list of code cells 600 include one or more code cells 602a-c. Typically, each code cell is a data structure [that] has one or more fields. Code cell 602 includes an opcode field 604 corresponding to an operation upon one or more operands 606." (col. 63, ll. 39-44) (emphasis omitted).

1d. Tye discloses:

> There are many ways in which the background system 34 in the embodiment of the code transformer 800 … intermixes the steps of translation and optimization. As a result, the IR upon which an optimization is performed can comprise any combination of source, target, and pseudocode instructions. Therefore, an optimization technique, such as data flow analysis, used in binary translation should be flexible enough to handle any form of the IR. (col. 64, ll. 1-29).

1e. Tye discloses: "The background optimizer 58 processes the list of code cells 600 to perform optimizations using a binary image as input. Generally, optimizations reduce execution time and reduce system resource requirements of a machine executable program." (col. 64, ll. 24-28).

PRINCIPLES OF LAW

Anticipation

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharm. Corp.*, 432 F.3d 1368, 1375 (Fed. Cir. 2005) (citing *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565 (Fed. Cir. 1992)).

ANALYSIS

Claims 1-57

Issue: Did the Examiner err in finding that Tye teaches or suggests "modifying the intermediate representation to more efficiently execute the

one or more instructions for processing the bit field data," as set forth in claim 1?

Appellant contends that the portion of Tye cited by the Examiner for teaching the above-noted limitation (*i.e.*, column 63, lines 20-22) (1) fails to mention bit field data and (2) fails to suggest that the intermediate representation is modified "'to more efficiently execute the one or more instructions for processing the bit field data'" (App. Br. 11).

The Examiner finds that Tye discloses that "a bit field is a common idiom used in computer programming to store a set of Boolean data type flags compactly, as a series of bits" (Ans. 12) (emphasis omitted).

In essence, the Examiner appears to find that Tye's programs/instructions inherently include bit fields. We agree. We note that "[i]t is well settled that a prior art reference may anticipate when the claim limitations not expressly found in that reference are nonetheless inherent in it. Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes, the claimed limitations, it anticipates." *In re Cruciferous Sprout Litig.,* 301 F.3d 1343, 1349 (Fed. Cir. 2002) (citations and internal quotation marks omitted). Here, we find that the programs/instruction sets necessarily include bit fields.

The Examiner further finds that "Appellant acknowledges that in Tye 'the intermediate representation is modified to produce a final version that corresponds to instruction[s] in the second instruction set'" (Ans. 14) (emphasis omitted). The Examiner also finds that Tye discloses an "optimization technique[,] such as data flow analysis used in binary

translation to handle any form of the IR (Intermediate Representation)" (Ans. 12).

In other words, Tye discloses instruction sets, creating an intermediate representation of the instruction sets, and an optimization technique for implementing the process. Specifically, in Tye the background translator builds an intermediate representation (IR), and then modifies the intermediate representation (*see* FF 1a). Tye further teaches that (1) the intermediate representations comprise one or more code cells 602 and (2) that a code cell 602 includes an opcode field 604 and one or more operands (*see* FF 1b and 1c). Tye further discloses that each code cell is a data structure that has one or more fields. We find that the opcode and the operand inherently includes components that occupy a bit field, and thus, both (*i.e.*, the opcode and operand) include bit field data. For example, as shown in Tye's Fig. 43, a CALL-Flag is generally used in instruction sets.

In addition, Tye discloses "optimizing" the executable program (*see* FF 1d-1e). We find that the claimed "to more efficiently execute the one or more instructions . . ." reads on Tye's optimization techniques. Even if it did not, which it does, we further find that the claimed "to more efficiently execute the one or more instructions . . ." is merely intended use language. An intended use of a claimed device does not limit the scope of the claim. *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997) (product claim's intended use recitations not given patentable weight); *see also Boehringer Ingelheim Vetmedica, Inc. v. Schering-Plough Corp.,* 320 F.3d 1339, 1345 (Fed. Cir. 2003) ("An intended use or purpose usually will not limit the scope of the claim because such statements usually do no more than define a

context in which the invention operates."). Although "[s]uch statements often . . . appear in the claim's preamble," *In re Stencel,* 828 F.2d 751, 754 (Fed. Cir. 1987), a statement of intended use or purpose can appear elsewhere in a claim. *Id.* Thus, we need not give the above-noted recitation regarding "to more efficiently …" any patentable weight.

Accordingly, we find that the Examiner did not err in finding that Tye teaches "modifying the intermediate representation to more efficiently execute the one or more instructions for processing the bit field data," as set forth in claim 1. Thus, for at least the reasons discussed *supra*, we find the Examiner did not err in rejecting representative claim 1 under 35 U.S.C. § 102, and claims 2-57 which fall therewith.

DECISION

The Examiner's rejection of claims 1-57 under 35 U.S.C. § 102(b), as being anticipated by Tye, is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv) (2009).

AFFIRMED

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